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# U.S. PATENT APPLICATION

**for**

# LOW-TEMPERATURE, LOW-RESISTIVITY HEAVILY DOPED P-TYPE POLYSILICON DEPOSITION


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# LOW-TEMPERATURE, LOW-RESISTIVITY HEAVILY DOPED P-TYPE POLYSILICON DEPOSITION

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application is a divisional of Herner et al., US Patent Application No. 10/441,601, "Low-Temperature, Low-Resistivity Heavily Doped P-Type Polysilicon Deposition," which is hereby incorporated by reference in its entirety.

## BACKGROUND OF THE INVENTION

**[0002]** The invention relates to a method of depositing doped polycrystalline silicon, hereinafter referred to as polysilicon, at low temperature.

**[0003]** Thin doped polysilicon films are typically deposited at temperatures between 540 and 625 degrees C by low pressure chemical vapor deposition (LPCVD.) Alternatively, an amorphous silicon film can be deposited at lower temperatures with dopants, then annealed after deposition at temperatures of 550 degrees C or greater to crystallize the silicon and activate the dopants. In general, as deposition temperature drops, the deposition rate and quality of doped polysilicon films decreases.

**[0004]** The temperatures required to create doped polysilicon films using conventional methods are incompatible with other processes and materials that may be desirable. For example, aluminum metallization withstands a maximum practical fabrication temperature of only 475 degrees C for semiconductor processing.

**[0005]** Ishihara, US Patent No. 5,956,602, "Deposition of Polycrystal Si Film," discloses a method to deposit a doped polysilicon film at temperatures below 500 degrees C. This method introduces a source gas like $SiH_4$ and a dopant gas such as $BCl_3$, $PH_3$, or $Al(CH_3)_3$. The two gases are flowed at different times, without overlapping. Hydrogen

plasma is then used to anneal the film. The process is repeated until a film of the desired thickness is produced.

**[0006]** While this method claims to produce doped polysilicon at temperatures below 500 degrees C., it has disadvantages. Repeatedly introducing the source and dopant gases at different times and annealing with hydrogen plasma involves significant process complexity and requires specialized equipment. Further, alternately introducing the silicon and dopant source gases may result in dopant nonuniformities throughout the film.

**[0007]** There is a need, therefore, to create high-quality doped polysilicon films at temperatures less than those used in conventional processes and that do not require a subsequent high temperature anneal. It would be preferable if complex deposition cycles and specialized equipment are not required.

## SUMMARY OF THE INVENTION

**[0008]** The present invention is defined by the following claims, and nothing in this section should be taken as a limitation on those claims. In general, the invention is directed to a method to deposit low-resistivity doped polysilicon at low temperatures.

**[0009]** According to one aspect of the invention, a method for depositing a doped polysilicon film comprises providing a surface and substantially simultaneously flowing $SiH_4$ and $BCl_3$ over the surface at a temperature less than or equal to about 500 degrees Celsius under conditions that achieve an average concentration in the doped polysilicon film of between about $7 \times 10^{20}$ and about $3 \times 10^{21}$ boron atoms per cubic centimeter.

**[0010]** According to another aspect of the invention, a method for forming in-situ doped polysilicon comprises providing a surface and substantially simultaneously flowing a first source gas comprising $SiH_4$ and a second source gas comprising $BCl_3$ over the surface at a temperature less than about 500 degrees Celsius under conditions sufficient to achieve in the doped polysilicon an average concentration of between about $7 \times 10^{20}$ and about $3 \times 10^{21}$ boron atoms per cubic centimeter.

**[0011]** A related embodiment provides for a semiconductor device comprising in-situ doped polysilicon formed by a method comprising providing a surface, and substantially simultaneously flowing $SiH_4$ and $BCl_3$ over the surface at a temperature less than about 500 degrees Celsius, wherein an average concentration of boron atoms in the polysilicon of between about $7x10^{20}$ and about $3 x10^{21}$ per cubic centimeter is achieved.

**[0012]** Another related embodiment provides for a monolithic three dimensional memory comprising polysilicon formed by a method comprising substantially simultaneously flowing $SiH_4$ and $BCl_3$ at a temperature less than or equal to about 500 degrees Celsius, wherein an average concentration of boron atoms in the polysilicon is between about $7 \times 10^{20}$ and about $3 \times 10^{21}$ per cubic centimeter, wherein the monolithic three dimensional memory comprises two or more memory levels.

**[0013]** A preferred embodiment provides for a method for depositing in-situ doped polysilicon, the method comprising providing a surface comprising a substantially horizontal surface and a substantially vertical sidewall descending from the horizontal surface, the sidewall having a top, and depositing an in-situ doped polysilicon film on the surface at a temperature less than about 500 degrees Celsius, wherein a first thickness of the film at its thinnest point on the vertical sidewall is at least 80 percent of a second thickness of the film on the sidewall at the top of the sidewall, and a third thickness of the film on the horizontal surface is at least 200 angstroms.

**[0014]** Another preferred embodiment provides for an in-situ doped polysilicon film wherein the polysilicon film was deposited at a temperature less than about 500 degrees Celsius, and the polysilicon film is deposited by substantially simultaneously flowing a first source gas comprising $SiH_4$ and a second source gas comprising $BCl_3$, wherein the polysilicon film has a sheet resistance less than about 280 ohms/square.

**[0015]** Other preferred embodiments are provided, and each of the preferred embodiments can be used alone or in combination with one another.

**[0016]** The preferred embodiments will now be described with reference to the attached drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0017]** FIGs. 1a through 1c illustrate decreasing quality of P+ polysilicon film at progressively lower deposition temperatures.

**[0018]** FIG. 2 is a graph showing sheet resistance of polysilicon films vs. deposition temperature for different dopant concentrations.

**[0019]** FIG. 3 is a graph showing deposition rate in angstroms per minute vs. deposition temperature for different dopant concentrations.

**[0020]** FIGs. 4a through 4c illustrate film step coverage over uneven surfaces.

## DETAILED DESCRIPTION OF THE INVENTION

**[0021]** A challenge of semiconductor device design is to select materials that are thermally compatible. If a deposition or anneal process requires high temperatures, other materials already present must be compatible with those temperatures.

**[0022]** Doped polysilicon has many uses in the semiconductor industry. For many designs and devices, it would be advantageous to deposit a low-resistance doped polysilicon film with good step coverage at low temperature. Specifically, it would be useful to form a low-resistance doped polysilicon film with good step coverage at temperatures below about 500 degrees. Aluminum wiring is used in many integrated circuit designs, but when used with doped polysilicon, the aluminum can only be deposited after the doped polysilicon is deposited and in a low resistivity state, since aluminum will soften and/or extrude at temperatures above about 475 degrees C, making practical semiconductor fabrication difficult. Thus even lower temperatures for deposition of doped polysilicon, for example about 475 degrees and below, would also

highly advantageous. By employing methods according to the present invention, aluminum wiring, for example, could be formed *before* doped polysilicon deposition, then low-resistance doped polysilicon formed later, at temperatures low enough to avoid damaging the aluminum structures.

**[0023]** At about 550 degrees C, heavily doped p-type (P+) deposited silicon doped in situ (by providing dopant atoms during deposition, rather than by implanting them later) is polycrystalline and conductive and has low resistivity. This is in contrast to heavily doped n-type silicon, which tends to be amorphous at this deposition temperature, and must be annealed at a temperature of, for example, about 550 degrees C or greater to crystallize the silicon and render it conductive.

**[0024]** As temperature falls below 550 degrees C, however, the rate of deposition of P+ polysilicon generally decreases and the quality of the film begins to degrade. FIG. 1a is a scanning electron microscope image of a high-quality P+ polysilicon film 200 nm thick deposited by flowing $SiH_4$, $BCl_3$ and helium at 550 degrees C. In FIG. 1b, at a temperature of 500 degrees C, it can be seen a 200 nm thick film is rougher; this film will have higher resistivity. FIG. 1c shows a 200 nm thick P+ polysilicon film deposited at 460 degrees C. This film is very rough and discontinuous and would not be suitable for uses requiring a conductive film. In FIGs. 1a, 1b, and 1c, the concentration of boron atoms (a p-type dopant) in the polysilicon film is $2x10^{20}$ atoms/cm$^3$, a fairly typical dopant concentration for heavily doped polysilicon.

**[0025]** FIG. 2 shows sheet resistance for P+ in-situ doped polysilicon films deposited at different temperatures. It will be seen on curve A that for boron concentrations of 2 x $10^{20}$ atoms/cm$^3$, sheet resistance generally increases as deposition temperature decreases. In some applications the lowest possible sheet resistance is advantageous for device performance.

**[0026]** Deposition of P+ polysilicon has been achieved at low temperatures using $Si_2H_6$ and $B_2H_6$ as source gases, but there are disadvantages associated with use of these source gases. $B_2H_6$ tends to dope surfaces nonuniformly. Dopant concentration thus

tends to be highly nonuniform across the wafers in a reactor, and even across each wafer. Better uniformity is achieved using $B_2H_6$ at lower temperatures. However, at lower deposition temperatures, films deposited using $Si_2H_6$ and $B_2H_6$ are amorphous. Amorphous films require a high temperature anneal to make the film conductive. Further, $Si_2H_6$ is less commonly used in semiconductor fabrication than is $SiH_4$, and thus more expensive and less readily available.

**[0027]** It has largely been assumed that low-temperature deposition of P+ polysilicon using $SiH_4$ and $BCl_3$ without use of hydrogen plasma anneal or complex deposition cycles is impractical. The present application discloses, however, that by flowing very high amounts of $BCl_3$ with $SiH_4$, the deposition rate and film quality of P+ polysilicon at low temperatures can be significantly improved.

**[0028]** Briefly, by providing a surface and substantially simultaneously flowing $SiH_4$ and $BCl_3$ over the surface at a temperature less than or equal to 500 degrees Celsius, under conditions that achieve an average concentration in the doped polysilicon film of between about $7 \times 10^{20}$ and about $3 \times 10^{21}$ boron atoms/cm$^3$, a polysilicon film having a sheet resistance less than about 280 ohms per square can be achieved. Referring again to FIG. 2, it will be seen that at deposition temperature below 500 degrees, even as low as 460 degrees, the sheet resistance for a film with a boron concentration of $7 \times 10^{20}$ atoms/cm$^3$ (as shown on curve B) ranges between about 200 and below about 280 ohms/square.

**[0029]** As FIG. 2 shows, for concentrations of $2x10^{20}$ and $7x10^{20}$ boron atoms/cm$^3$, sheet resistance generally increases with decreasing deposition temperature below about 520 degrees Celsius. It is suspected that this increase may be due to decreased activation of the dopant.

**[0030]** FIG. 3 is a graph showing deposition rate of silicon in angstroms per minute at various deposition temperatures. Curve D shows deposition rates for undoped silicon, curve E for in-situ doped silicon with an average dopant concentration of $2x10^{20}$ boron atoms/cm$^3$, curve F for in-situ doped silicon with an average dopant concentration of

$7x10^{20}$ boron atoms/$cm^3$, and curve G for in-situ doped silicon with an average dopant concentration of $2x10^{21}$ boron atoms/$cm^3$. For all curves, the source gas providing silicon was $SiH_4$; in the doped cases, the source gas providing boron atoms comprised $BCl_3$. The gases were flowed substantially simultaneously. Helium was used to dilute $BCl_3$ and as a mixing gas for $SiH_4$ and $BCl_3$.

**[0031]** It will be seen that at a given temperature, the deposition rate generally increases as the dopant concentration increases.

**[0032]** Deposition for the points shown on curves D, E, F, and G took place at 400 mTorr. $SiH_4$ was flowed at 500 standard cubic centimeters per minute (sccm) and helium, an inert gas, at 700 sccm. For the depositions on curve E, in which the average dopant concentration was $2x10^{20}$ boron atoms/$cm^3$, 0.5 percent $BCl_3$ (balance helium) was flowed substantially simultaneously in addition to the $SiH_4$ and helium. For the depositions on curve F and G, in which the average dopant concentrations were $7x10^{20}$ boron atoms/$cm^3$ and $2x10^{21}$ boron atoms/$cm^3$ respectively, 1.5 percent $BCl_3$ (balance helium) was flowed substantially simultaneously in addition to the $SiH_4$ and helium.

**[0033]** Preferred embodiments of the present invention will now be described in more detail.

**[0034]** In a preferred embodiment, a substrate having a surface is placed in a reactor. P+ polysilicon formed according to the present invention may be deposited on any material to which it adheres, for example silicon dioxide. At temperatures less than or equal to about 500 degrees C, source gases $SiH_4$ and $BCl_3$ are substantially simultaneously flowed over the surface under conditions sufficient to achieve in the doped polysilicon an average concentration of between about $7 \times 10^{20}$ and about $3 \times 10^{21}$ boron atoms/$cm^3$.

**[0035]** The temperature during deposition is preferably between about 450 and about 480 degrees, more preferably between about 460 and 475 degrees.

**[0036]** Many possible flow conditions will produce in-situ doped polysilicon of the named dopant concentrations. Pressure is preferably between about 200 mTorr and about 1 Torr, more preferably about 400 mTorr. Above about 1 Torr, the risk of gas-phase nucleation increases, which will prevent formation of a satisfactory film, though the risk decreases with lower temperature.

**[0037]** At least two source gases will be substantially simultaneously flowed. For two or more gases to be "substantially simultaneously" flowed means that the gases are flowed at the same time during the deposition, the flows overlapping. It is not essential that the flows of both gases start or end at the same instant. The first source gas comprises $SiH_4$. Preferably the first source gas is $SiH_4$. In a preferred embodiment, $SiH_4$ is flowed at about 400 sccm.

**[0038]** Using conventional equipment, very low flows of gas can be difficult to control. The second gas could be pure $BCl_3$, but to improve uniformity and flow control, the second gas is preferably $BCl_3$ mixed with an inert gas, such as helium, argon, or nitrogen; preferably helium. The second source gas thus comprises $BCl_3$. The second source gas may also comprise an inert gas, which may be helium. The percentage of $BCl_3$ in the second source gas may be as low as 0.1 percent. In a preferred embodiment, a mixture of about 1.5 percent $BCl_3$ and the balance helium is flowed at about 10 sccm.

**[0039]** As noted, the flows, temperature, and the concentrations of $SiH_4$ (in the first source gas) and $BCl_3$ (in the second source gas) should be selected to achieve a concentration of boron atoms in the polysilicon film averaging between about $7x10^{20}$ and about $3x10^{21}$ boron atoms/$cm^3$.

**[0040]** The following table details flow of $BCl_3$ in sccm used to deposit doped polysilicon at concentrations of $7x10^{20}$ boron atoms/$cm^3$ and at $2x10^{21}$ boron atoms/$cm^3$ for different deposition temperatures:

| Deposition Temperature degrees C | 1.5% $BCl_3$ sccm, ccn= $7x10^{20}/cm^3$ | 1.5% $BCl_3$ sccm, ccn= $2x10^{21}/cm^3$ |
|---|---|---|
| 460 | 10 | 20 |
| 490 | 18 | 36 |
| 520 | 34 | 68 |
| 550 | 62 | 124 |
| 580 | 114 | 228 |

**[0041]** In general, as temperature drops, more boron atoms will be incorporated, so the skilled practitioner will adjust other aspects of deposition conditions, including flows, concentrations, and pressures, accordingly, as a matter of routine experimentation.

**[0042]** In addition to the first source gas comprising $SiH_4$ and the second source gas comprising $BCl_3$, flowing an inert gas, such as helium, argon, or nitrogen, can improve mixing and lead to more uniform dopant concentrations across a wafer and across wafers in a reactor. In a preferred embodiment, helium is flowed at about 700 sccm.

**[0043]** More generally, the concentration of boron atoms in the film is correlated with the ratio of $SiH_4$ to $BCl_3$. To increase the concentration of boron atoms in the film, for example, the skilled practitioner will change the ratio by decreasing $SiH_4$ (by decreasing concentration or flow) or increasing $BCl_3$ (by increasing concentration or flow.)

**[0044]** Preferred embodiments of P+ polysilicon deposited according to the method of the present invention provide an additional advantage in that such polysilicon has excellent step coverage. It is common in semiconductor processing to coat uneven surfaces with a deposited layer. If a material has good step coverage, it can be deposited over uneven surfaces, for example over trenches, and will cover horizontal surfaces at the top and bottom of the trenches, and vertical sidewalls of trenches, with a substantially uniform thickness.

**[0045]** Poor step coverage can make it difficult or impossible to fill a high-aspect ratio trench or via. As shown in Fig. 4a, during chemical or vapor deposition an

overhang 16 may form at the opening of the trench. This results in a shadowing effect, sheltering the lower sidewalls and bottom of the via from further deposition and causing a void if the lip "pinches off" and closes.

**[0046]** As shown in FIG. 4b, in-situ doped polysilicon formed according to the present invention can be deposited with good sidewall and bottom coverage, and without tending to pinch off and form voids if deposited over a trench, by avoiding formation of a significant overhang. Specifically, for a P+ polysilicon film 18 formed according to the present invention, at temperatures below about 500 degrees, deposited over a substantially vertical sidewall 20 descending from a substantially horizontal surface 22, the thickness 24 at its thinnest point on sidewall 20 of the film 18 will be at least 80 percent of the thickness 26 of film 18 on the sidewall 20 at the top of the sidewall, when thickness 28 of the film 18 on horizontal surface 22 is at least 200 angstroms. "Thickness" here is presumed to be measured perpendicular to the sidewall or surface, whichever is named. If the level of fill is above the top of the sidewall, then the thickness at the thinnest point will be the same as the thickness at the top of the sidewall, unless there are any voids; in this case the thinnest point will be measured from the void, as in FIG. 4c. Overhang is undesirable whether or not the vertical sidewall is a trench sidewall.

**[0047]** In-situ doped polysilicon formed according to the present invention can be used in any semiconductor devices or arrays of devices, including memory arrays, that are advantageously formed at low temperature. Examples of such devices include, but are not limited to, logic or memory devices, transistors formed in monocrystalline silicon, thin-film transistors (in which polysilicon could form a portion of a channel), capacitors, resistors, inductors, diodes, interconnects, PROMs, EPROMs, and EEPROMs. One such semiconductor device may comprise portions of a diode separated by an antifuse which become a diode when the antifuse is ruptured. Arrays of such devices include, but are not limited to, two dimensional and monolithic three dimensional arrays.

**[0048]** P+ polysilicon formed according to the present invention could be advantageously used in monolithic three dimensional memories such as those described

in Johnson et al., US Patent No. 6,034,882, "Vertically stacked field programmable nonvolatile memory and method of fabrication"; Johnson, US Patent No. 6,525,953, "Vertically stacked field programmable nonvolatile memory and method of fabrication"; Knall et al., US Patent No. 6,420,215, "Three Dimensional Memory Array and Method of Fabrication"; Lee et al., US Patent Application No. 09/927648, "Dense Arrays and Charge Storage Devices, and Methods for Making Same," filed August 13, 2001; and Herner et al., US Patent Application No. 10/326470, "An Improved Method for Making High-Density Nonvolatile Memory," filed December 19, 2002, all hereby incorporated by reference. P+ polysilicon formed according to the present invention can be used whenever P+ or doped polysilicon is called for in any of the patents or applications name herein.

**[0049]** Monolithic three dimensional memories present particular challenges for temperature compatibility of processing. In simpler, conventional two dimensional structures (without stacked memory levels), it's possible to combine doped polysilicon, requiring temperatures over 550 degrees C, and aluminum, requiring temperatures not exceeding 475 degrees C, if the doped polysilicon is formed at higher temperatures first, then aluminum metallization is formed later.

**[0050]** In contrast, in monolithic three dimensional memories, a memory level, including all of its associated metallization, is formed, and then another memory level is formed above it. This means that all elements of a memory level (including, for example, aluminum metallization) are subjected to the temperatures required to form every element (including, for example, low-resistance polysilicon) of the next level. Low-temperature formation of low-resistance polysilicon in one memory level offers the advantage that it does not damage aluminum metallization, or other structures with low temperature tolerances, that already exist in a previously-formed level. Thus a low-temperature method to form in-situ doped polysilicon can be particularly useful in monolithic three-dimensional memories.

EXAMPLE

**[0051]** In one example, P+ polysilicon according to the present invention was formed on silicon wafers in an ASML RVP 9000. The ASML RVP 9000 has a capacity of 176 wafers. Every other slot was filled, so 88 wafers were used at an effective pitch of 8.6 mm. Of these 88 wafers, only 75 were product wafers, centered vertically; the rest were dummy wafers. The product wafers had previously had a layer of oxide deposited on them, and P+ polysilicon was deposited on the oxide. The remainder of the wafers were dummy wafers coated with a protective silicon nitride film to prevent breakage, as described in Herner et al., "Dummy Wafers and Methods for Making the Same," US Patent Application No. 10/036291, filed November 7, 2001, hereby incorporated by reference. The pressure was stabilized at 400 mTorr and the temperature at 460 degrees C. $SiH_4$ was flowed at 500 sccm, helium was flowed at 700 sccm, and 1.5 percent $BCl_3$ (balance helium) was flowed at 10 sccm to deposit 2000 angstroms of P+ polysilicon.

**[0052]** The foregoing detailed description has described only a few of the many forms that this invention can take. For this reason, this detailed description is intended by way of illustration, and not by way of limitation. It is only the following claims, including all equivalents, which are intended to define the scope of this invention.